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Design of a faster 8T SRAM memory cell

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A R T I C L E I N F O

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A B S T R A C T

This paper discusses the design of read/write assist circuits which are used in a SRAM cell's design to overcome the cell's variations. It also explains the variability problems in a SRAM bit-cell and many approaches to address them. The basic operations, SNM concept, and write margin of an SRAM are described theoretically as well as measured in simulation. The write assisted circuit, the Negative Bit-line Voltage Bias scheme, is discussed and implemented at transistor level using a six-transistor (6T) SRAM cell. With the write assisted circuit, the implemented memory array successfully performs a write operation, the condition in which the same operation would fail without the write assisted circuit. During the simulation, this write assisted circuit helps to achieve the negative bias voltage of -70mV on the SRAM's bit- lines. The cost overhead includes chip area, power consumption and chip area.

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Introduction:

Moore's law predicts that the number of transistors that can be placed on an integrated circuit is doubled approximately every two years. In parallel, the need for bit counts in an embedded Static Random Access Memory (SRAM) has been growing exponentially. Thus, the probability of a defect in an embedded SRAM cell is constantly increasing. In addition, as the process technology continues to scale, the stability of an embedded SRAM cell is not only a major design consideration, but also a concern for testing as well. [1-3].

SRAM cell's designers encounter many challenges as technology scales. First of all, it has become increasingly complicated to maintain an acceptable Static Noise Margin (SNM) in a SRAM cell while scaling the minimum size and supply voltage. As a result, the control of the process parameters becomes exceedingly difficult, because the increased process variations are translated into a wider distribution of transistor and circuit characteristics. Secondly, it has been observed that there are many variability problems at a transistor level in the SRAM bit-cell. For example, as the Operating Voltage (VDDMIN) is reduced, it causes Read/Write/Access fails, or Data Retention fails. In addition there are other failures relating to variability in the SRAM cell's Sense Amplifier circuitry. Thirdly, tightly packaged chip areas can be especially susceptible and sensitive to manufacturing defects and process variations. For example, as large SRAM arrays are condensed to minimize their footprints in an integrated chip, they are more susceptible to defects. According to International Technology Roadmap for Semiconductors, it is predicted that "greater parametric yield loss with respect to noise margin" for high density circuits such as SRAM arrays, which are projected to occupy more than 90% of the SoC area in the next 10 years [4, 5].

To this end, this work will discuss a design of a SRAM cell and implementation of SRAM's related circuitry such as Read/Write assist circuits in order to address the discussed challenges in the current design of a SRAM cell. SRAM cell design in theory including SRAM cell architecture and basic operations of SRAM are briefly overviewed in section II. Finally, the proposed SRAM cell designs with a write

assist circuit are discussed in Section III. The paper also analyzes and compares the results of the simulated circuits

SRAM array architecture and block structure:

Figure 2.1 shows a typical small SRAM memory array architecture. In particular it is a block diagram of 64Kb SRAM memory array.

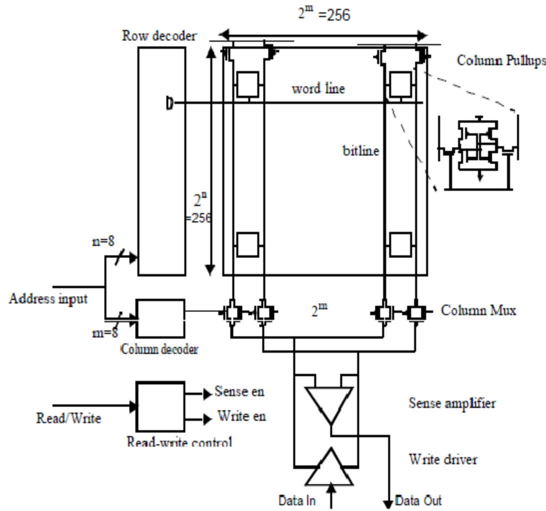


Fig. 1: Architecture of 64Kb SRAM.

In a simplest memory design, an array is organized with one row per word and one column per bit. There are far more words in the memory than bits in each word. This would lead to a very long and skinny memory architecture which is hard to fit in a floor plan or very slow because of a long bit line wire. Folding the rows to make more columns is the approach. There are a few major components in SRAM architecture as shown in Figure 2.1. They are row/column decoders, bit line conditioning, and column circuitry. The row decoder activates one particular row by inserting one of the word lines. Column decoder controls a multiplexer in the column circuitry from the row as the data to access. Bit-line conditioning circuitry helps to pre-charge bit lines before any SRAM operation. Finally, the column circuitry contains write drivers and read sensing circuits which are also called sense amplifiers.

Six-Transistor (6T) CMOS SRAM Cell:

The core storage element used for most register file and cache designs on high- performance microprocessors is a six-transistor CMOS cell with a single word-line and both true and complementary bit-lines. Figure 2.2 shows the circuit diagram of a 6T SRAM. The cell contains a pair of cross-coupled inverters and an access- transistor for each bit-line as combination read/write port. True and complementary versions of the data are stored on the cross-coupled inverters. If the data is disturbed slightly, positive feedback around the loop will restore it to VDD or GND. The word- line in inserted to read or to write the cell.

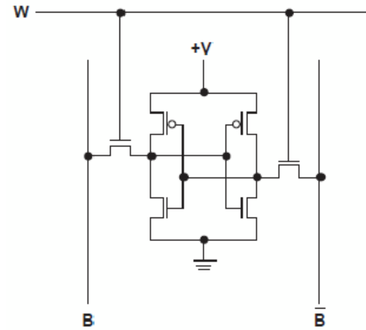


Fig. 2: Six-transistor SRAM cell.

SRAM Cell Operation:

SRAM operation can be divided into two phases, phase 1 - Φ1 and phase 2 - Φ2, which can be generated from clk and its complement clkb signals. Assume that the SRAM is pre-charged in phase 2. In phase 1, the SRAM is written, or read by raising the appropriate word line and either driving the bit lines to the value that should be written or leaving the bit lines floating and observing which one is pull down. The row and column are selected by row or column decoders. Reading a large SRAM array can be slow due the capacitance of the SRAM cells which are sharing the same bit line. This sense amplifier circuit (sense amp) can accelerate the read by detecting the differential voltage between the two complementary bit lines

READ operation:

Prior to initiating a read operation the two bit lines are pre-charged to VDD. The read operation begins by enabling the word line (word) and connecting the pre-charged bit lines, bit and bit_b, to the internal nodes of the cell. Figure 2.3 shows the data value of a 6T SRAM cell before a read operation

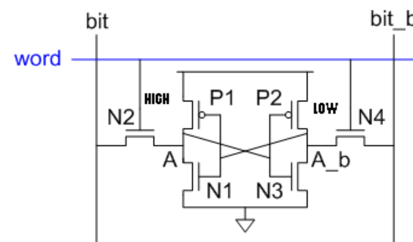


Fig. 3: 6T SRAM cell's initial condition before a Read/Write operation. Assume that the cell is currently storing logic "1"; node A (HIGH) is being held

At VDD by device P1 while node A_b (LOW) is being held at VSS by device N3. The series connection between turned ON device N3 and N4 allows the current to sink from the bit line node bit_b, therefore discharging it toward ground. Node HIGH stays the same at VDD because device P1 is ON and there is very little current flowing through. After a sufficient time a differential voltage developed on nodes bit and bit_b is detected by the sense amp circuit. This sense

amp circuit is activated and helps to further pull up and pull down the voltage the two bit lines bit and bit_b respectively. Finally the value that placed onto the bit lines is read.

WRITE operation:

The same as SRAM cell reading operation, the two bit lines are pre-charged to VDD in a write operation. The address decoder enables the word line (word) to open the two pass gates. Figure 2.3 shows a 6T SRAM cell's initial condition before a write operation, where the cell initially stored a logic "1"at node HIGH and is written with a logic "0" (Node HIGH is pulled down to Vss).

As discussed in a read operation, a minimum cell ratio is required to prevent undesired cell writing. Smaller cell ratios while preventing accidental updates also make it somewhat harder to accomplish a desired write operation. The read disturb condition which holds the internal node to a very low value. As a result, the inverter pair formed by device P2/N3 does not amplify the new write data and the high going side of the cell, does not contribute to the write operation of the cell.

The LOW going bit line (bit), also forms a voltage divider between the PMOS inverter P1 and pass gate N2. The pass gate must be much more conductive than the PMOS device for a write to the cell. The cell must be written by forcing A low through N2. P1 opposes this operation; thus P1 must be weaker than N2 so that A can be pulled low enough. This constraint called write-ability. Once A falls low, N3 turns OFF and P2 turns ON, pulling A_b high as desired.

READ assist circuits:

Read & Write-back method is an approach to provide data recovery by writing back the original data.Fig. 2.4 shows the read-assist schematic, which features a sense-amplifier (SA) integrated in each sub-array column. This read-assist circuit provides full Bit-Line (BL) amplification to the half-selected columns, which are idle columns during write or read operations. These half selected columns also contain unstable cells which are vulnerable during the half-selected operations. Full BL amplification improves the discharge rate of the low-node of the cell and provides the data recovery write back mechanism. As a result this discharge rate of the BL helps to reduce the failure of losing data on unstable cells when disturbed. If BLs, BLC0/BLT0, are written to during a write operation, BLs, BLC1/BLT1, are concurrently sensed and fully amplified. During the masking operation, bit-switch signals BSO and BS1 enable the sense-amplifier activation only on the selected column.

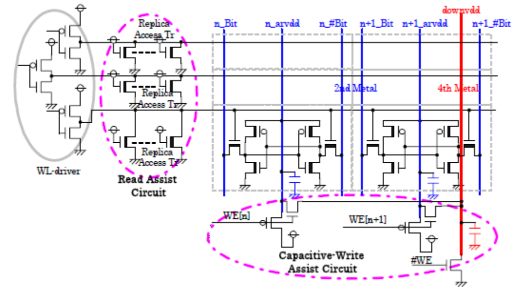


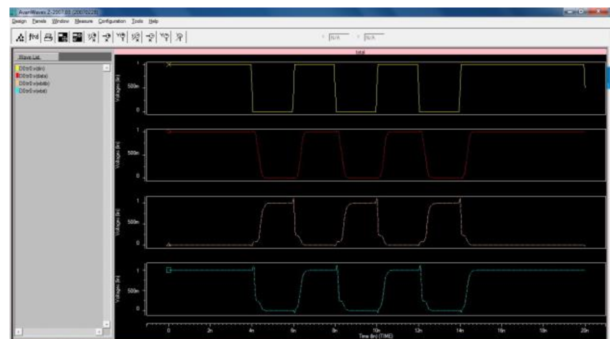
Fig. 2.4 Circuit diagram of a read-assist & write assist circuit

WRITE assist circuits:

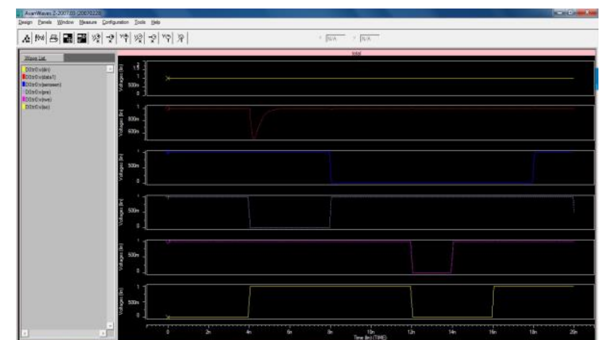
One of several write-assist circuits in an SRAM cell is a Lower VDD by column W-AC approach. Lowering an SRAM cell voltage Vdd level reduces the current to the pull-up pMOS device.

Simulation Results:

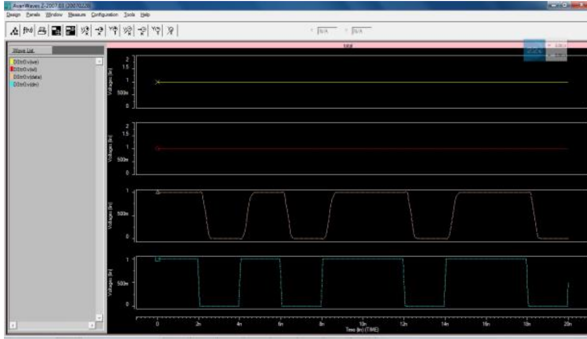
6T Read



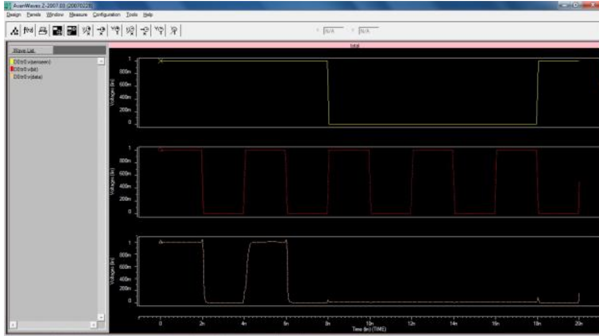
6T Write



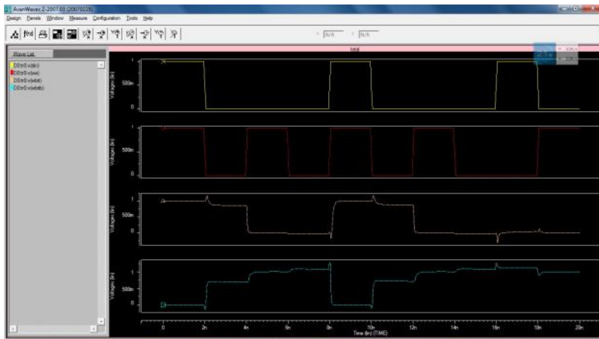
8T Read



8T Write



Sense amplifier read driver



Sense amplifier write driver

	6T SRAM		8T SRAM	
	POWER	DELAY	POWER	DELAY
WRITE	6.1×10^{-5}	3.6×10^{-10}	7.6×10^{-5}	3.6×10^{-10}
READ	6.9×10^{-5}	3.46×10^{-10}	7.1×10^{-5}	3.5×10^{-10}

	6T SRAM		8T SRAM	
	POWER	DELAY	POWER	DELAY
IDEAL	5.72×10^{-5}	NO DELAY	5.74×10^{-5}	NO DELAY

6T &8T SRAM

WRITE DRIVER CIRCUIT		READ DRIVER CIRCUIT (SENSE AMP)	
POWER	DELAY	POWER	DELAY
1.6×10^{-5}	1.42×10^{-10}	8.8×10^{-6}	1.1×10^{-10}

Conclusion:

For the implemented design the simulations were performed. Read, Write circuit timing diagrams of 8T SRAM cell have shown considerable improvement. Power and delay measurements show almost nearer values. Hence we could achieve higher architecture with good operation characteristics.

References:

1. Meixner and J. Banik. Weak write test model: An SRAM cell stability design for test technique. In Proc. IEEE International Test Conferrence (ITC), pages 1043-1052, November 1997.
2. D.-W. Kwai, H.-W. Chang, H.-J. Liao, C.-H. Chiao, and Y.-F. Chou. Detection of SRAM cell stability by lowering array supply voltage. In Proc of the Ninth Asian Test Symposium (ATS 2000), pages 268-273, December 2000.
3. C. Kou, T. Toms, B.T. Neel, J. Jelemensky, E.A. Carter, and P. Smith. Soft-defect detection (SDD) technique for a high-reliability CMOS SRAM. IEEE Journal of Solid-State Circuits (JSSC), 25:61-67, February 1990.